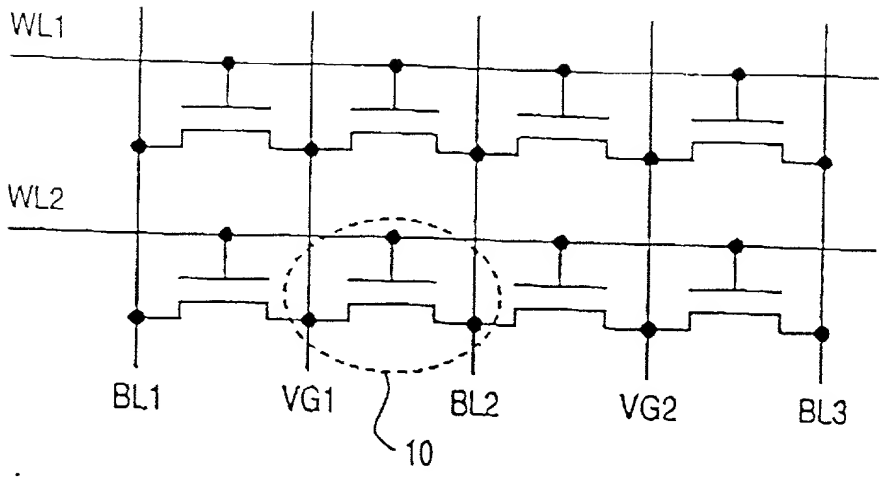


FIG. 1
(PRIOR ART)

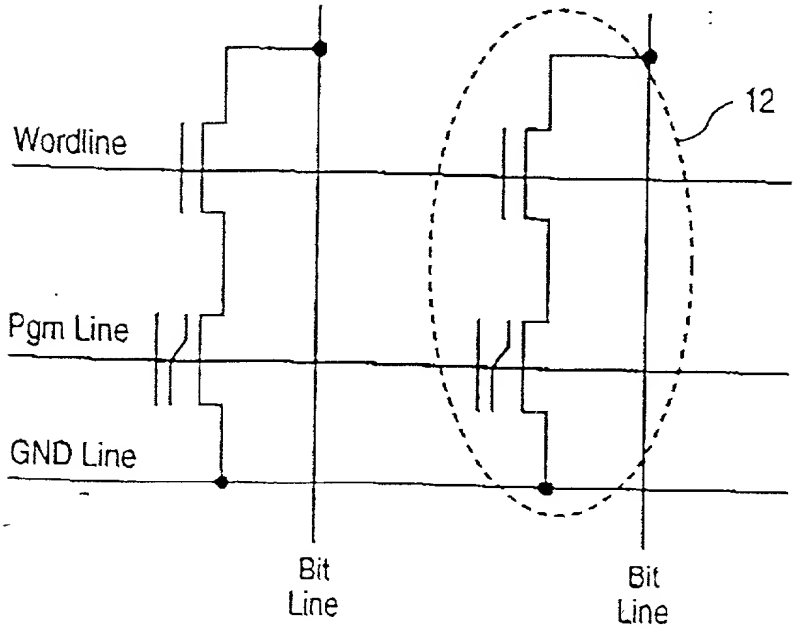


FIG. 2
(PRIOR ART)

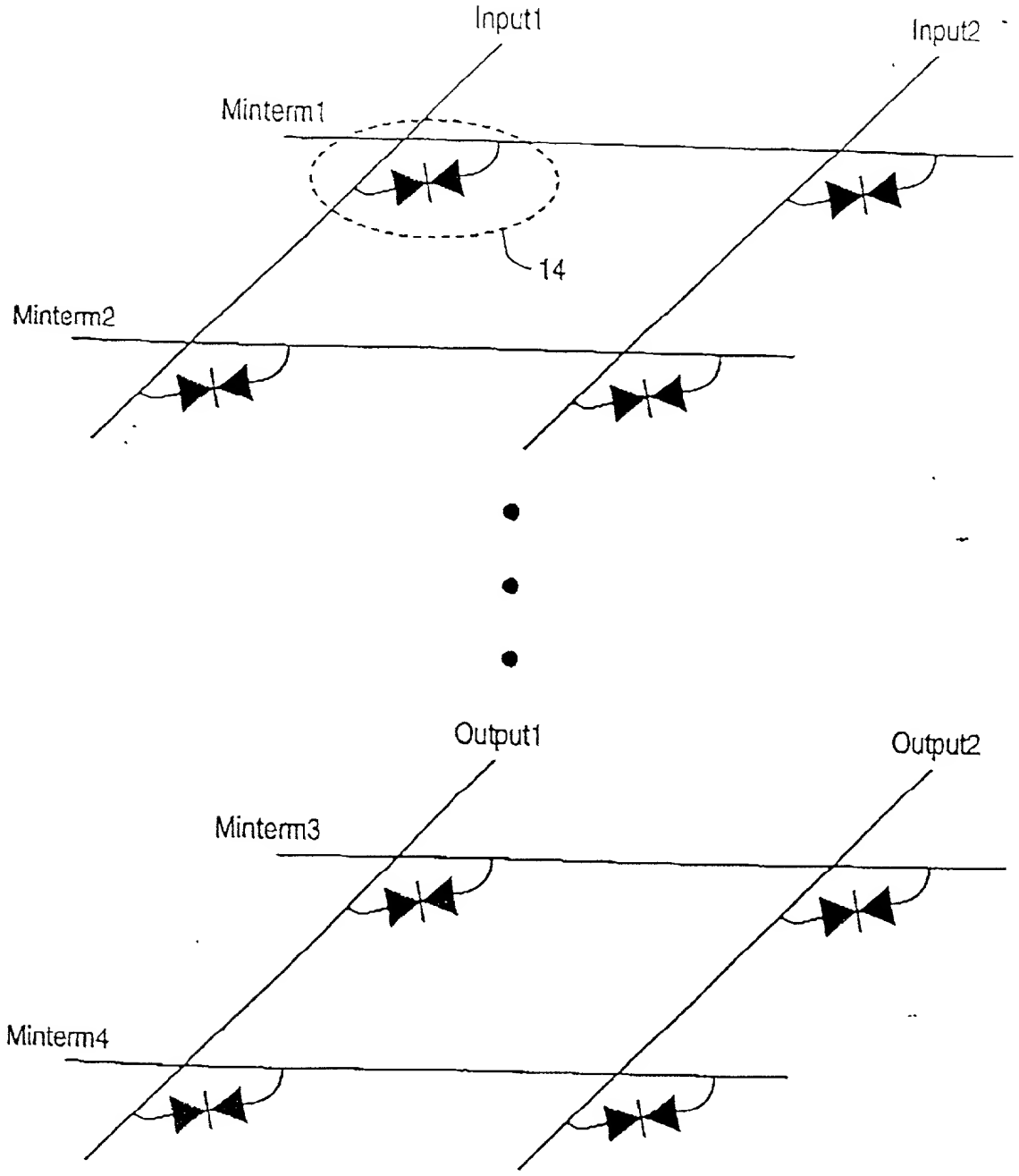


FIG. 3
(PRIOR ART)

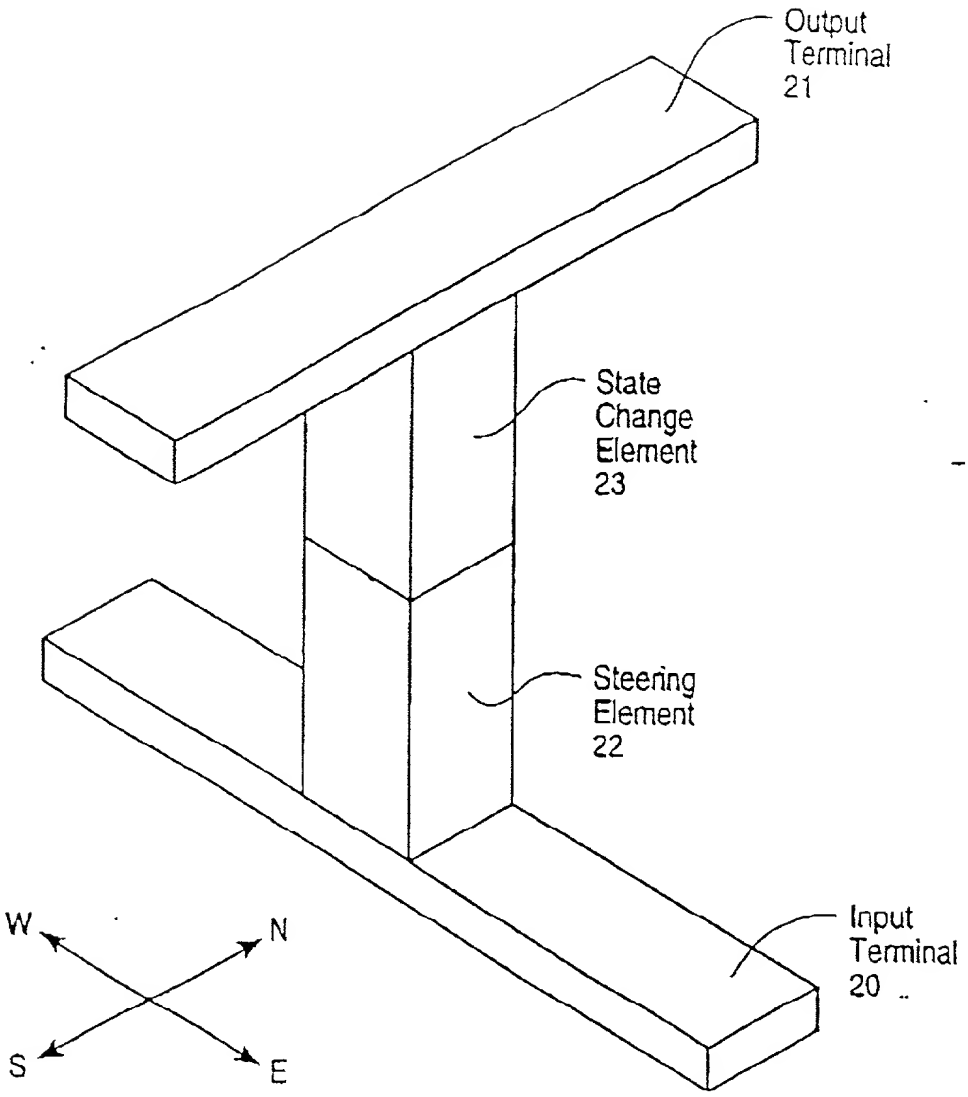

Output
Terminal
21
State
Change
Element
23
Steering
Element
22
Input
Terminal
20
W
N
S
E

FIG. 4(a)

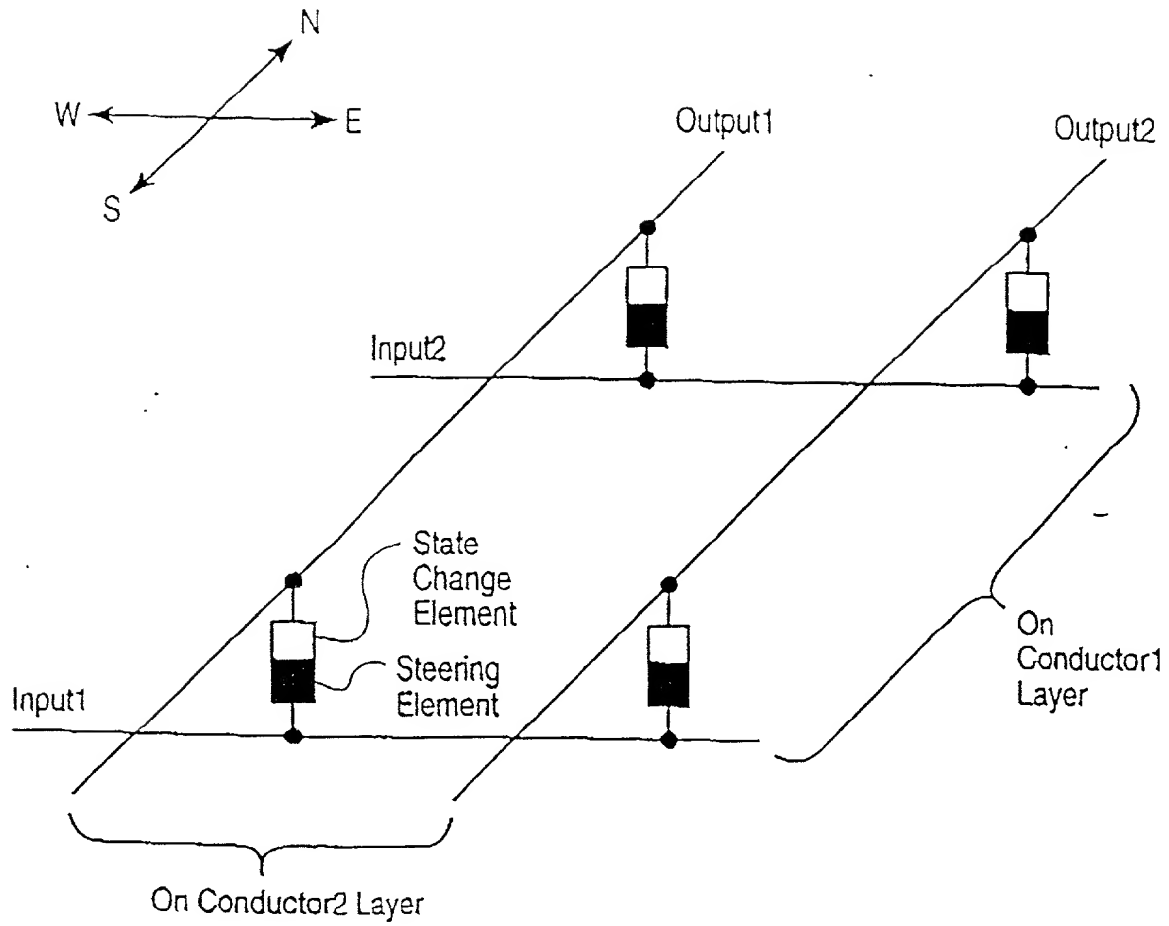

N
W
E
S
Output1
Output2
Input2
State
Change
Element
Steering
Element
Input1
On
Conductor1
Layer
On Conductor2 Layer

FIG. 4(b)

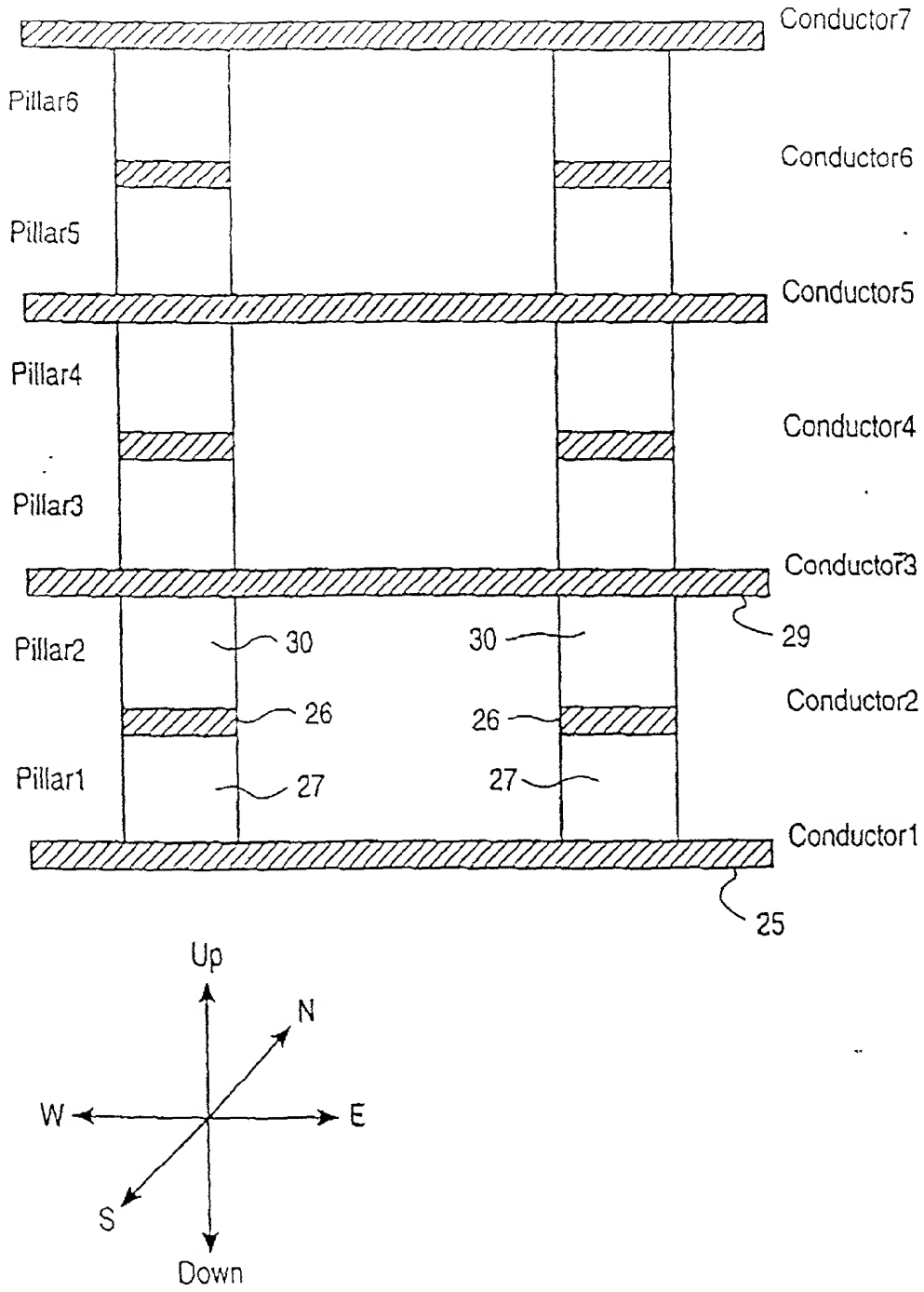

Conductor7
Pillar6
Conductor6
Pillar5
Conductor5
Pillar4
Conductor4
Pillar3
Conductor3
29
Pillar2
30
30
Conductor2
26
26
Pillar1
27
27
Conductor1
25
Up
N
W
E
S
Down

FIG. 5

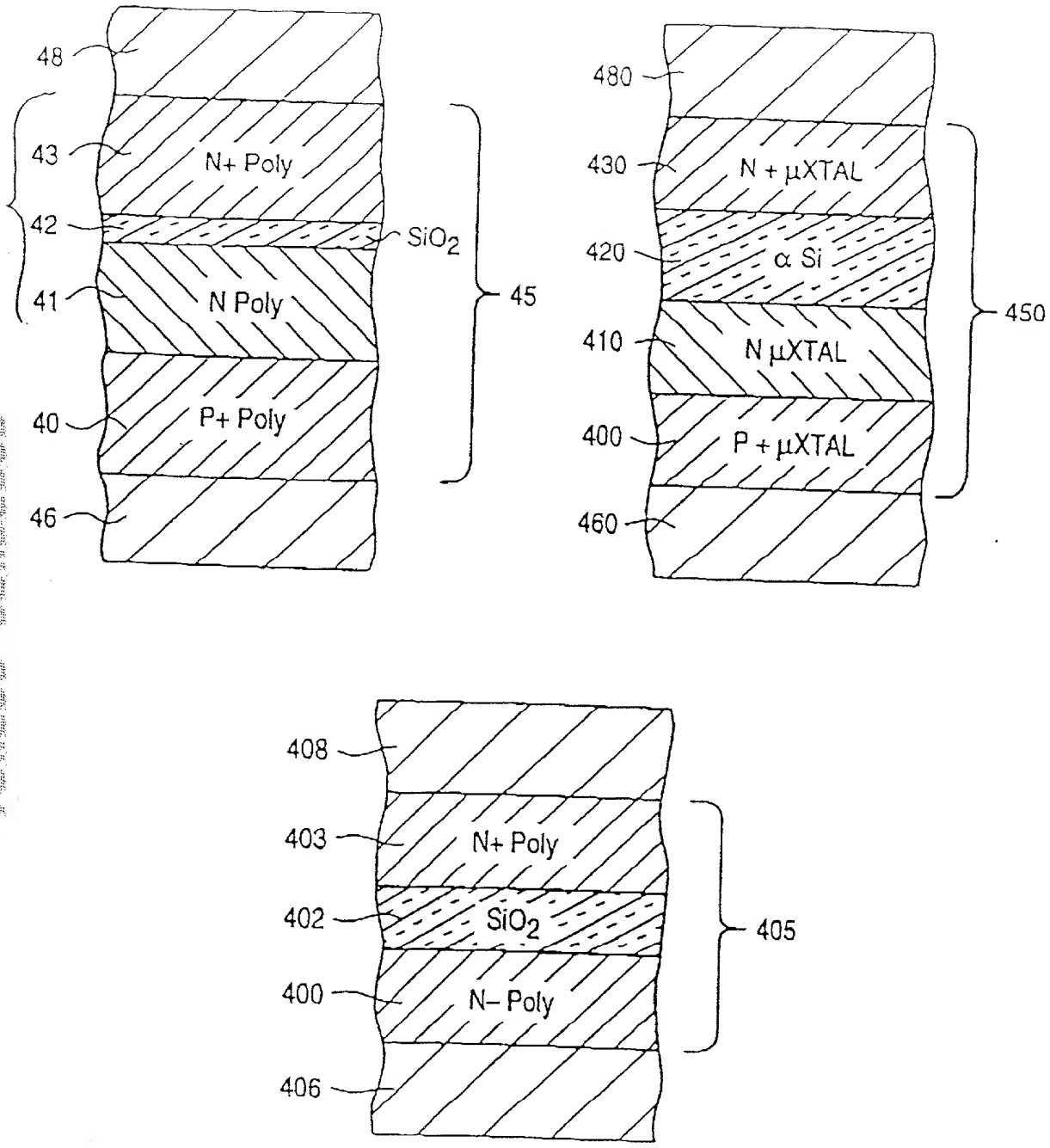

48
43
N+ Poly
42
SiO_2
41
N Poly
45
40
P+ Poly
46
480
430
N + μXTAL
420
α Si
450
410
N μXTAL
400
P + μXTAL
460
408
403
N+ Poly
402
SiO_2
405
400
N– Poly
406

FIG. 6(a)

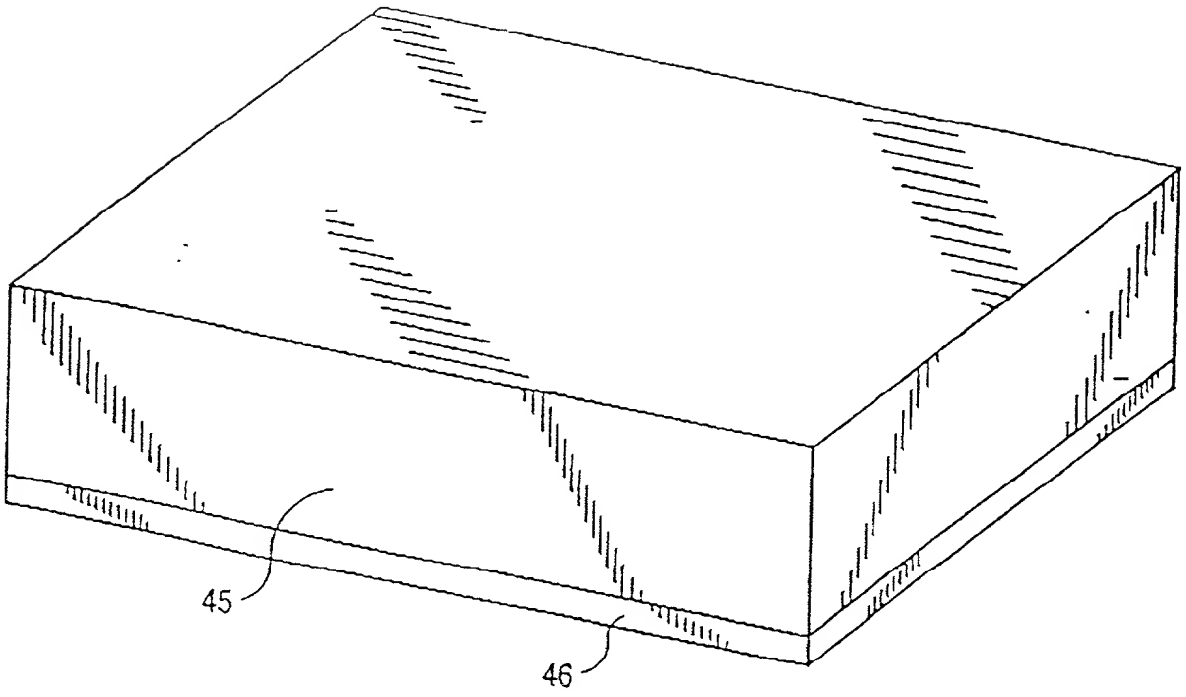


FIG. 6(b)

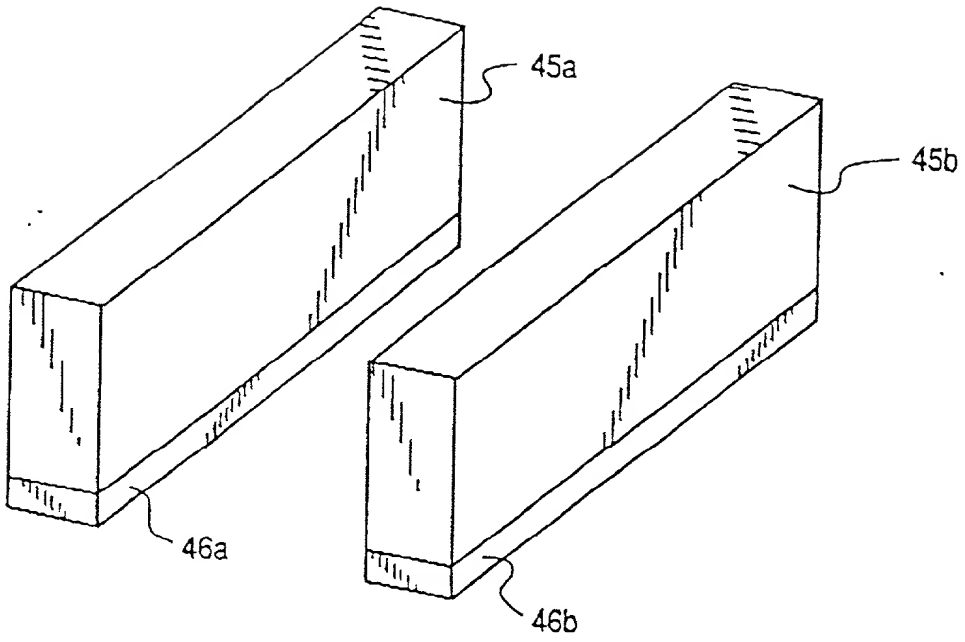


FIG. 6(c)

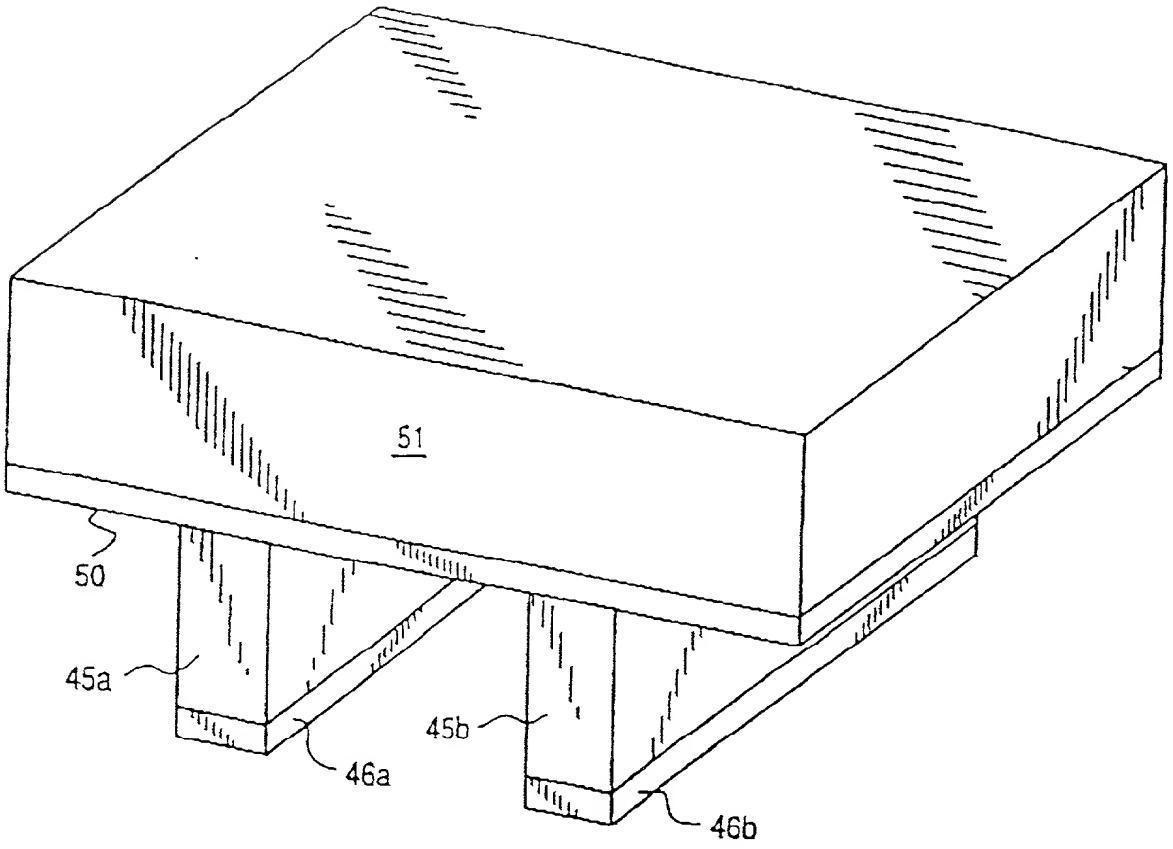


FIG. 6(d)

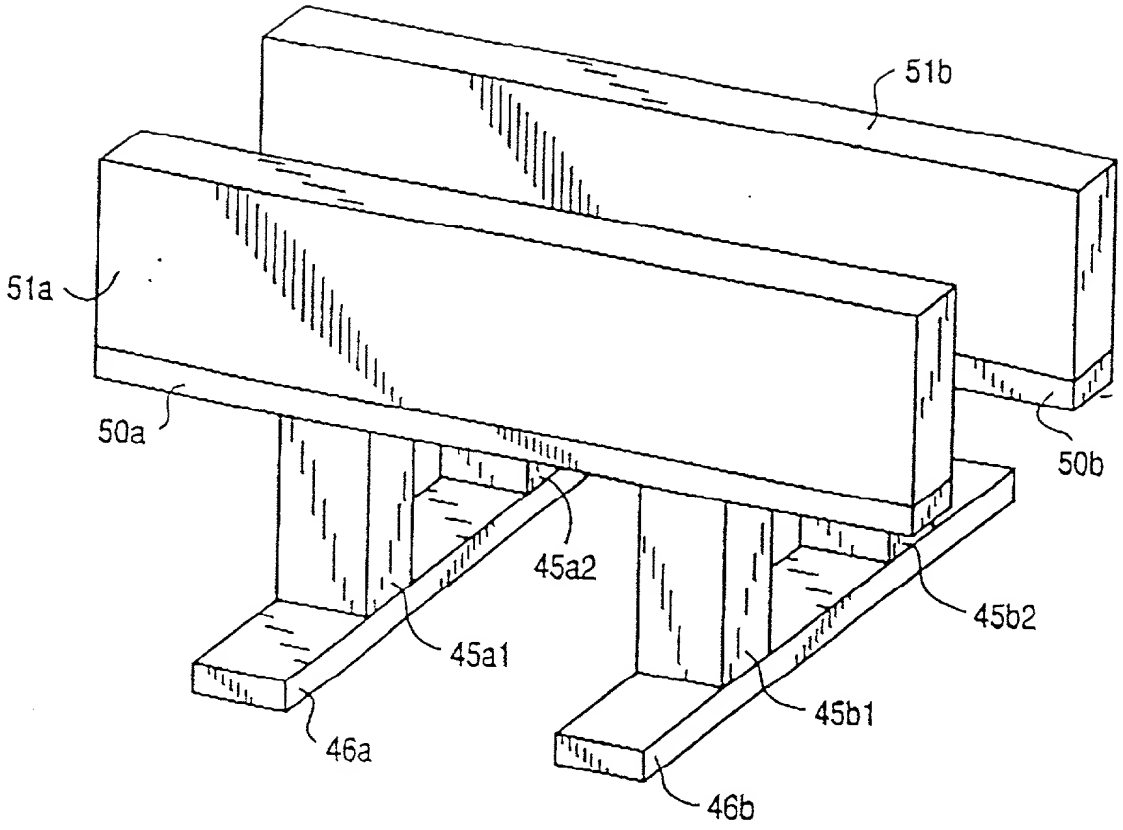


FIG. 6(e)

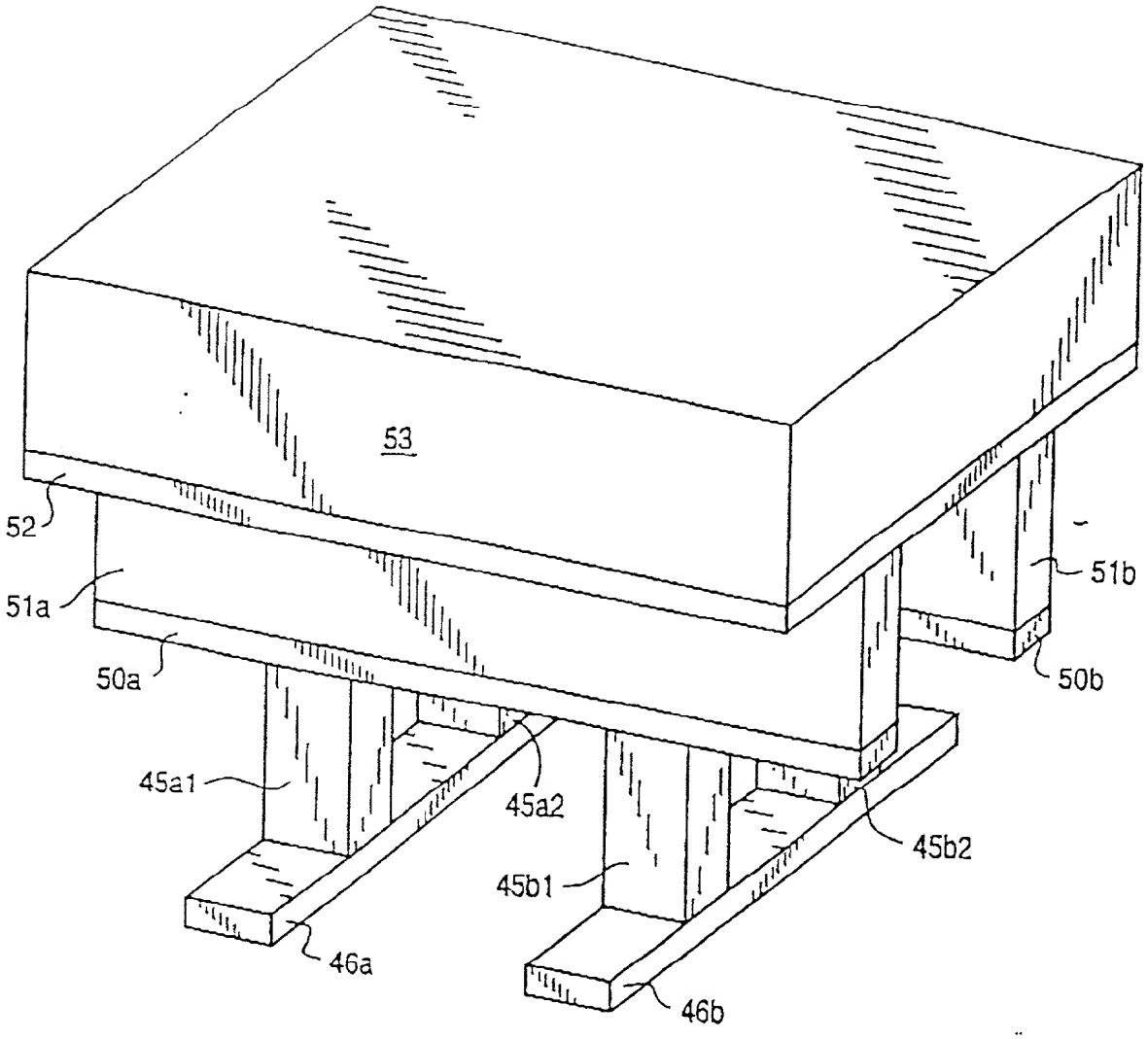


FIG. 6(f)

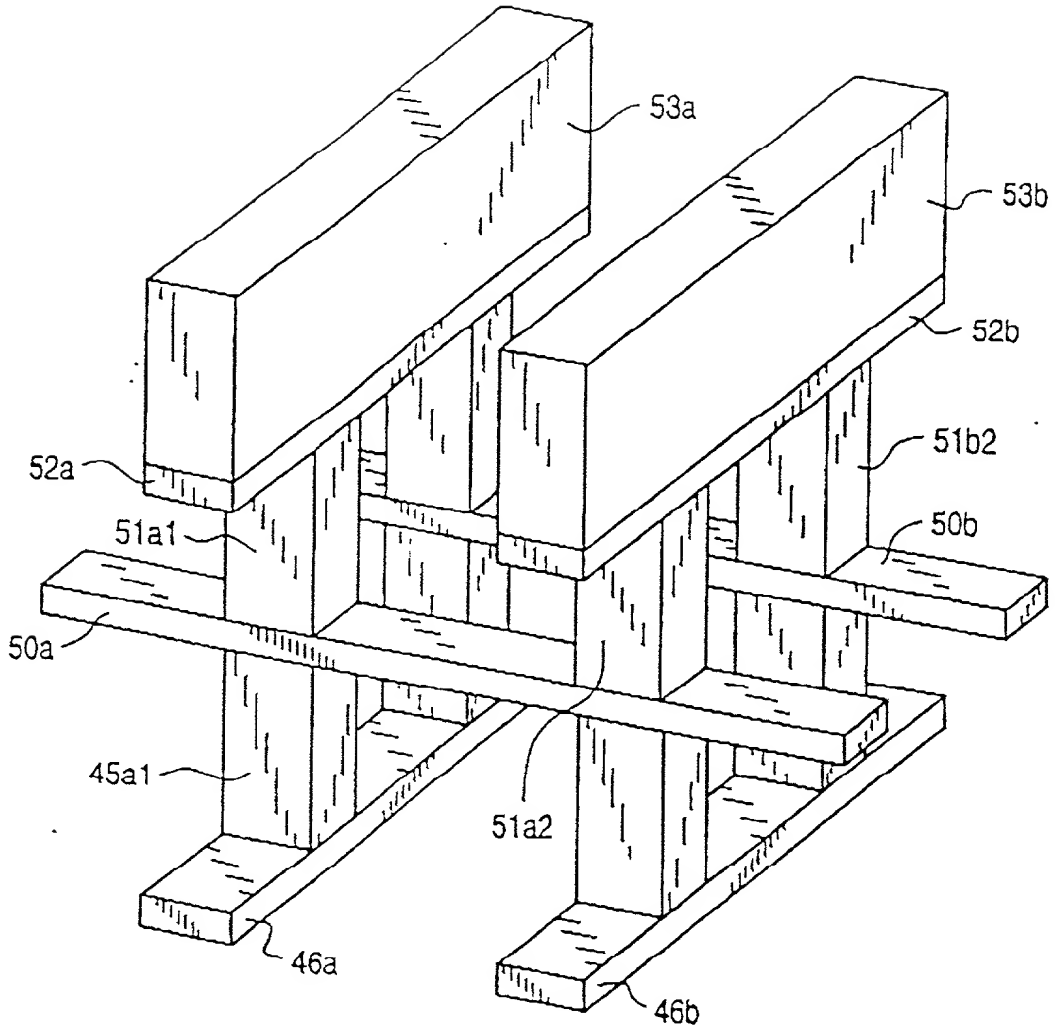
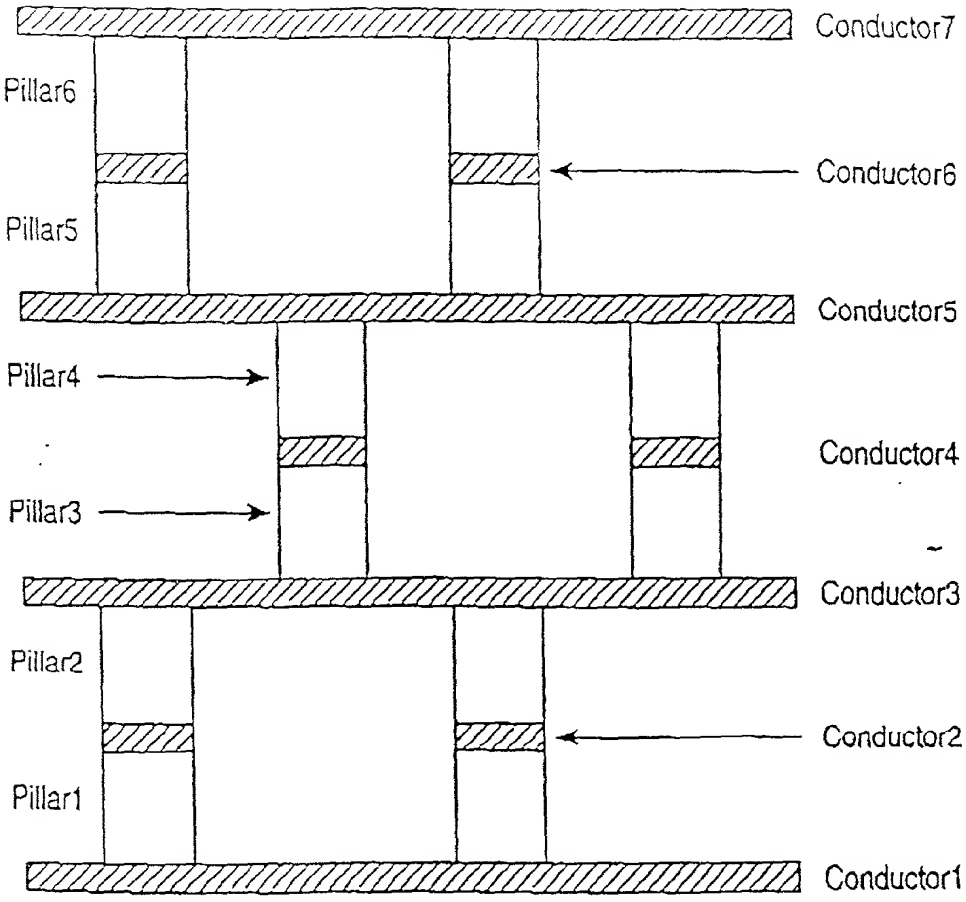


FIG. 6(g)


Conductor7
Pillar6
Conductor6
Pillar5
Conductor5
Pillar4
Conductor4
Pillar3
Conductor3
Pillar2
Conductor2
Pillar1
Conductor1

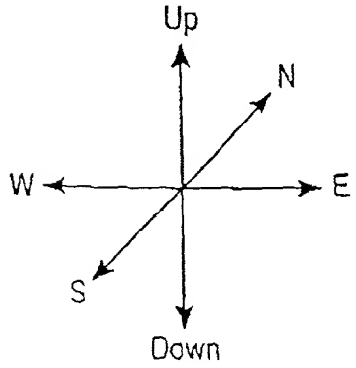

Up
N
W
E
S
Down

FIG. 7

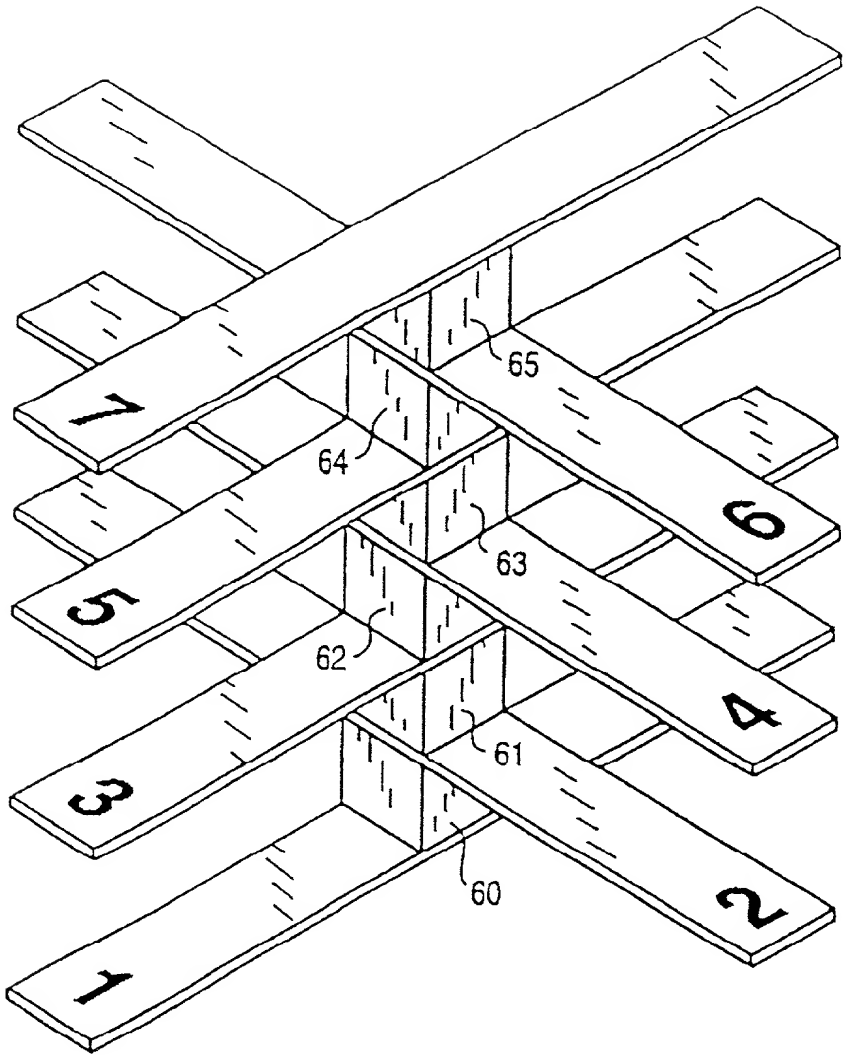


FIG. 8(a)

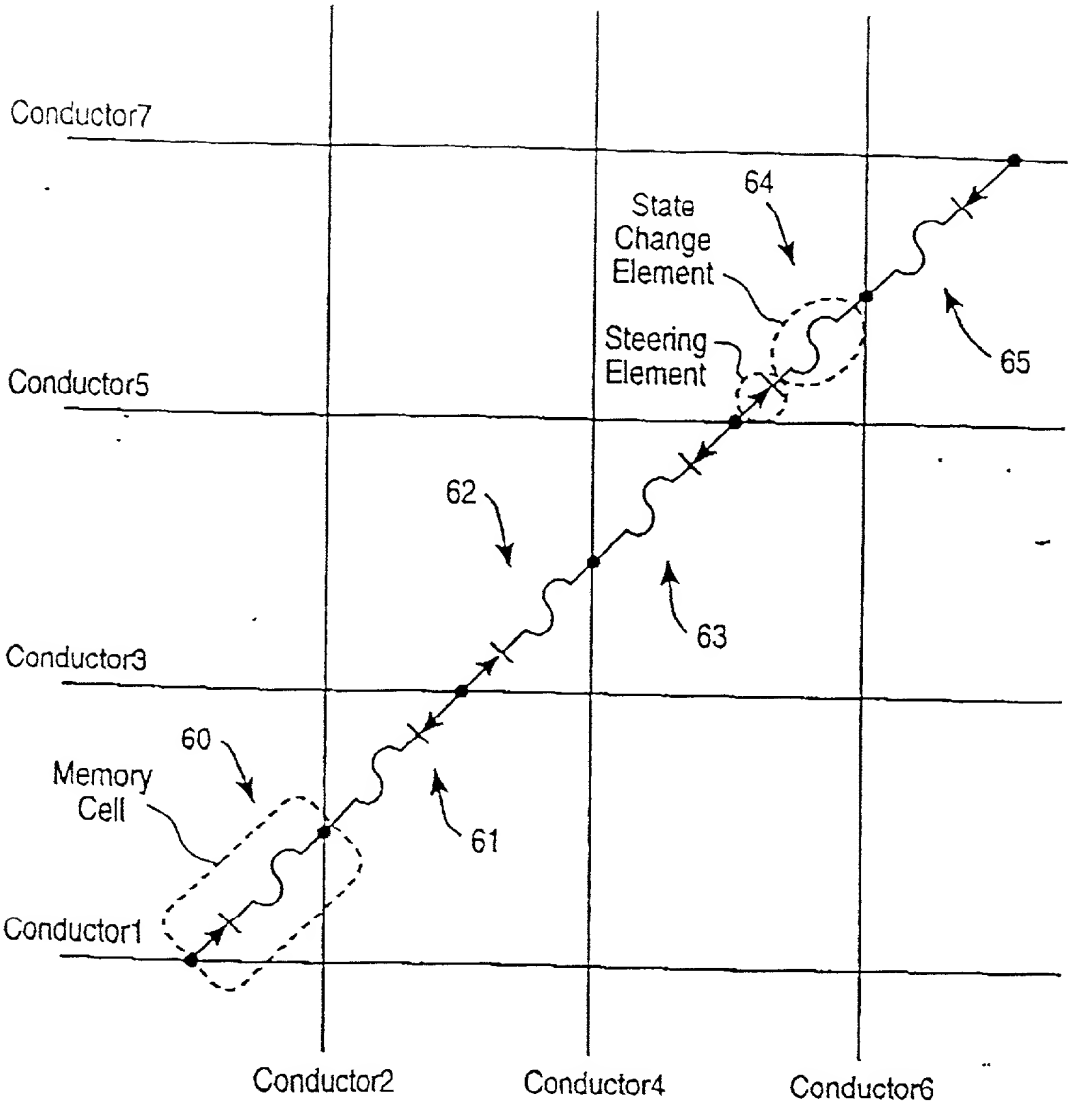

Conductor7
Conductor5
Conductor3
Conductor1
Conductor2
Conductor4
Conductor6
64
State
Change
Element
Steering
Element
65
62
63
60
Memory
Cell
61

FIG. 8(b)

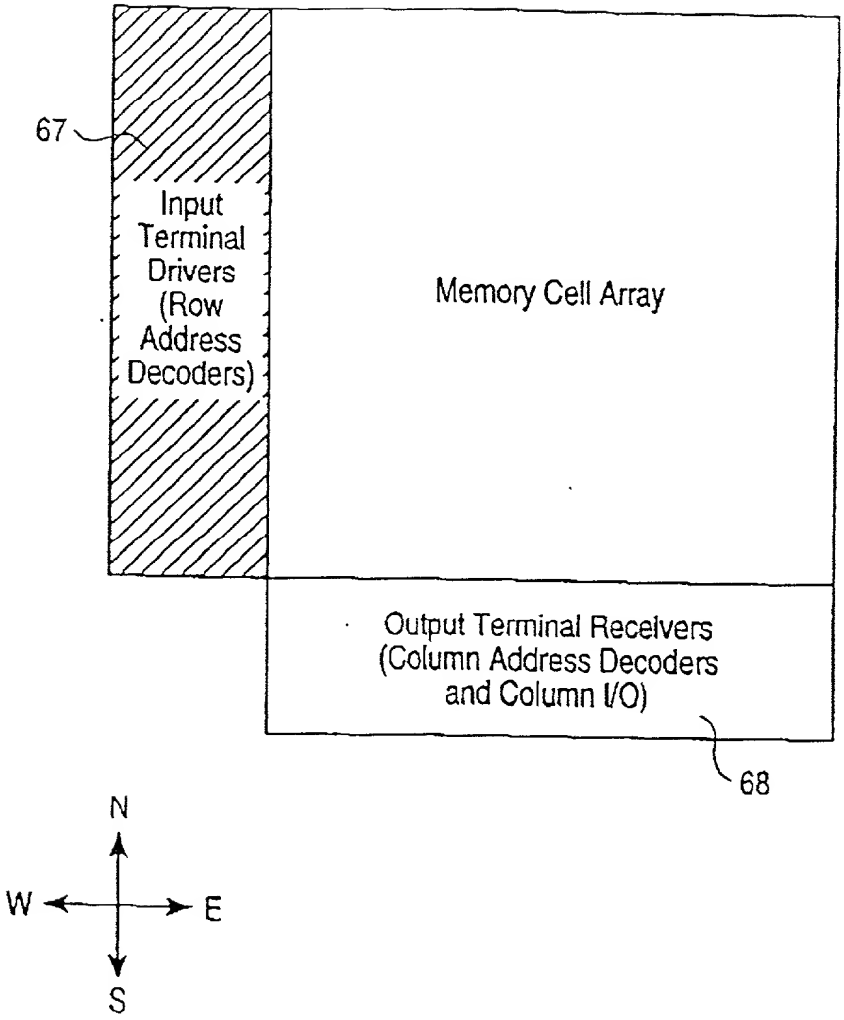

67
Input Terminal Drivers (Row Address Decoders)
Memory Cell Array
Output Terminal Receivers (Column Address Decoders and Column I/O)
68
N
W
E
S

FIG. 9(a)

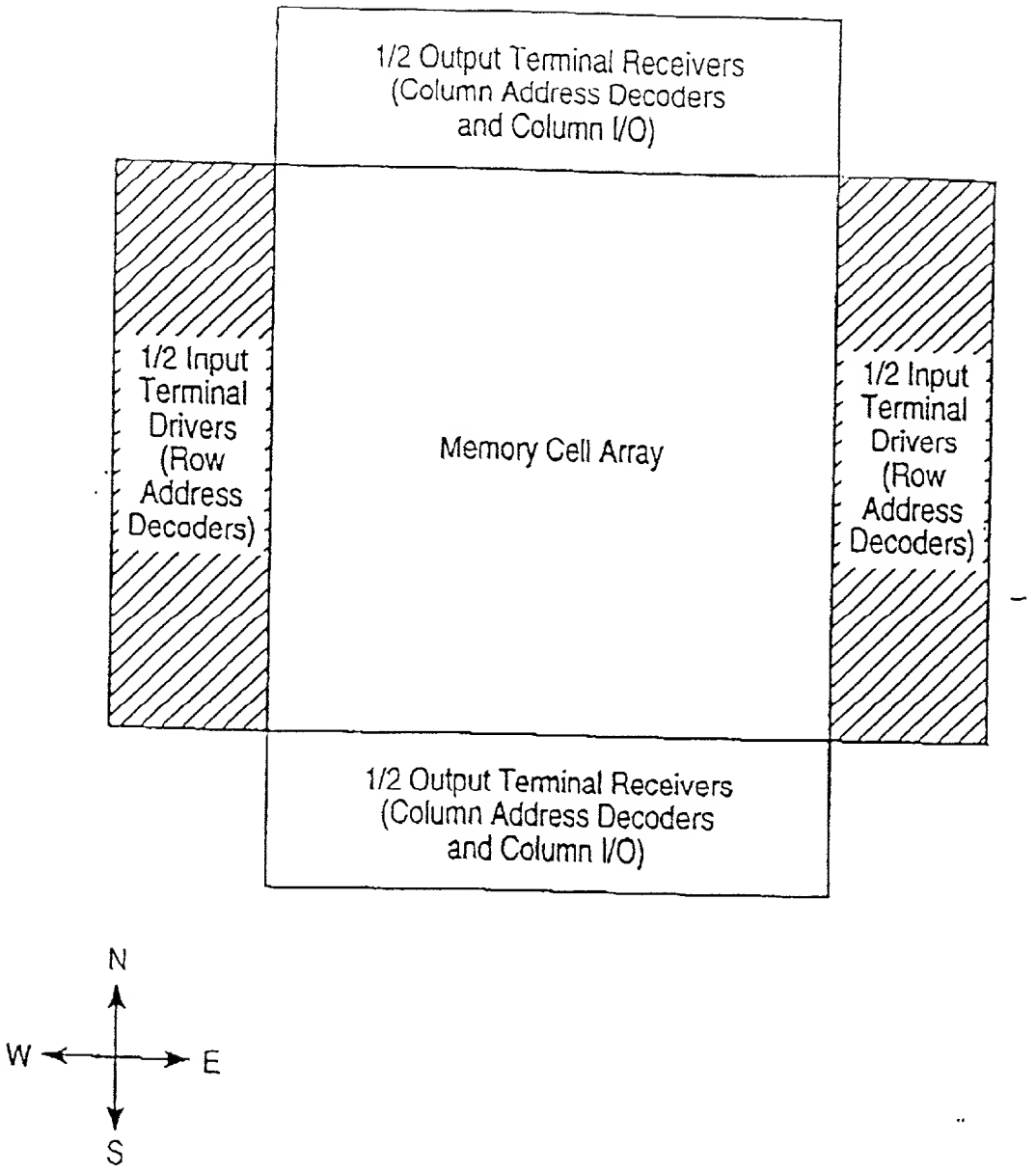

1/2 Output Terminal Receivers
(Column Address Decoders
and Column I/O)
1/2 Input
Terminal
Drivers
(Row
Address
Decoders)
Memory Cell Array
1/2 Input
Terminal
Drivers
(Row
Address
Decoders)
1/2 Output Terminal Receivers
(Column Address Decoders
and Column I/O)
N
W
E
S

FIG. 9(b)

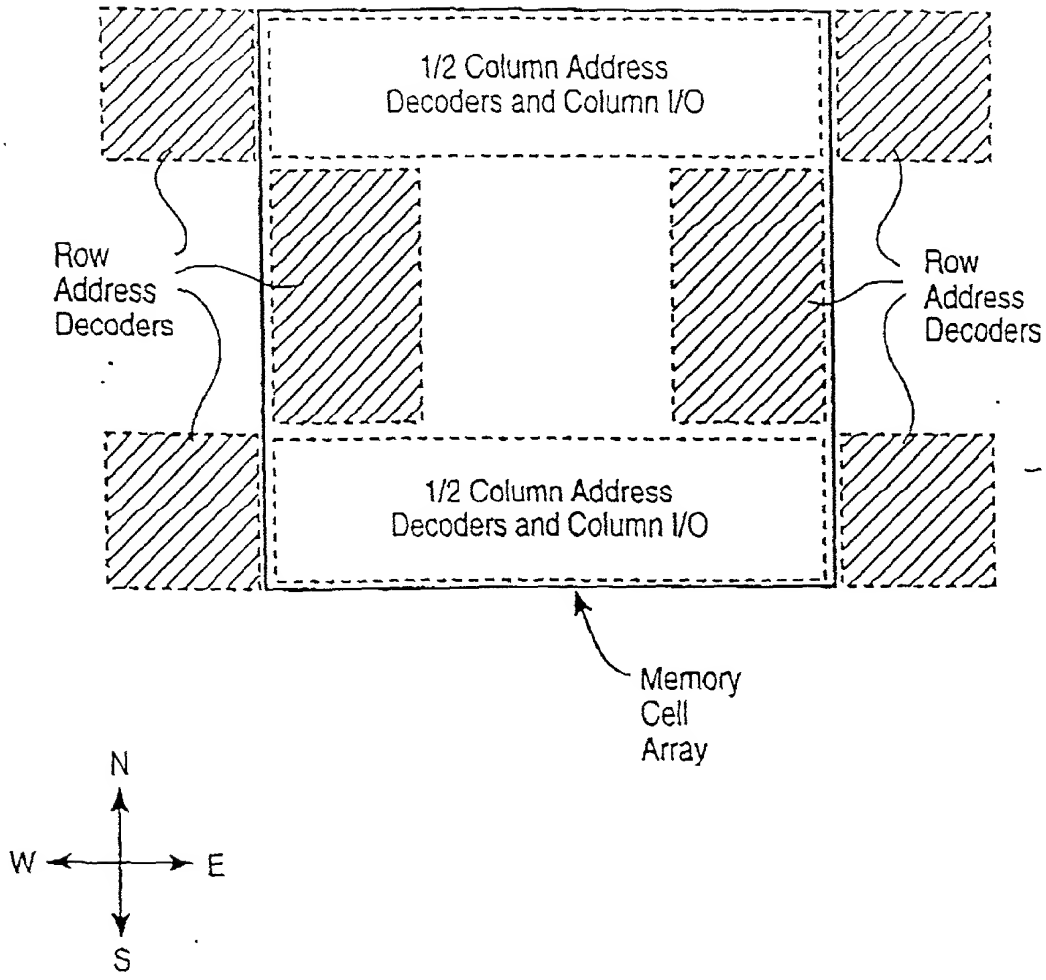

1/2 Column Address
Decoders and Column I/O
Row
Address
Decoders
Row
Address
Decoders
1/2 Column Address
Decoders and Column I/O
Memory
Cell
Array
N
W
E
S

FIG. 9(c)

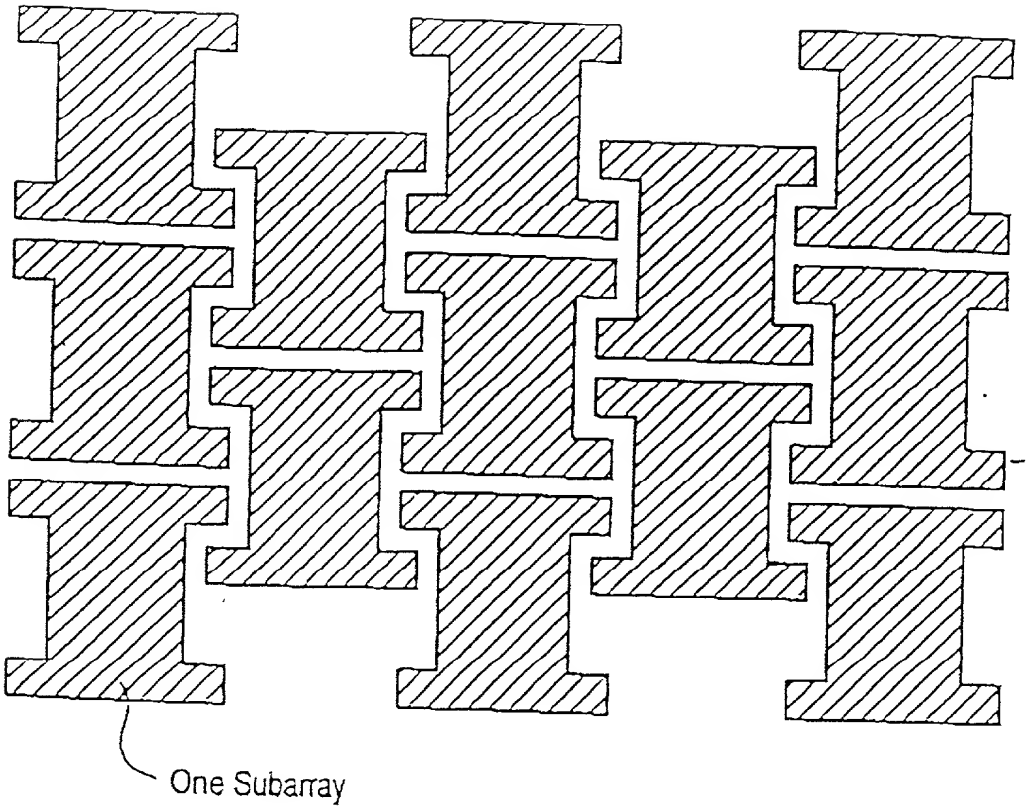


FIG. 9(d)

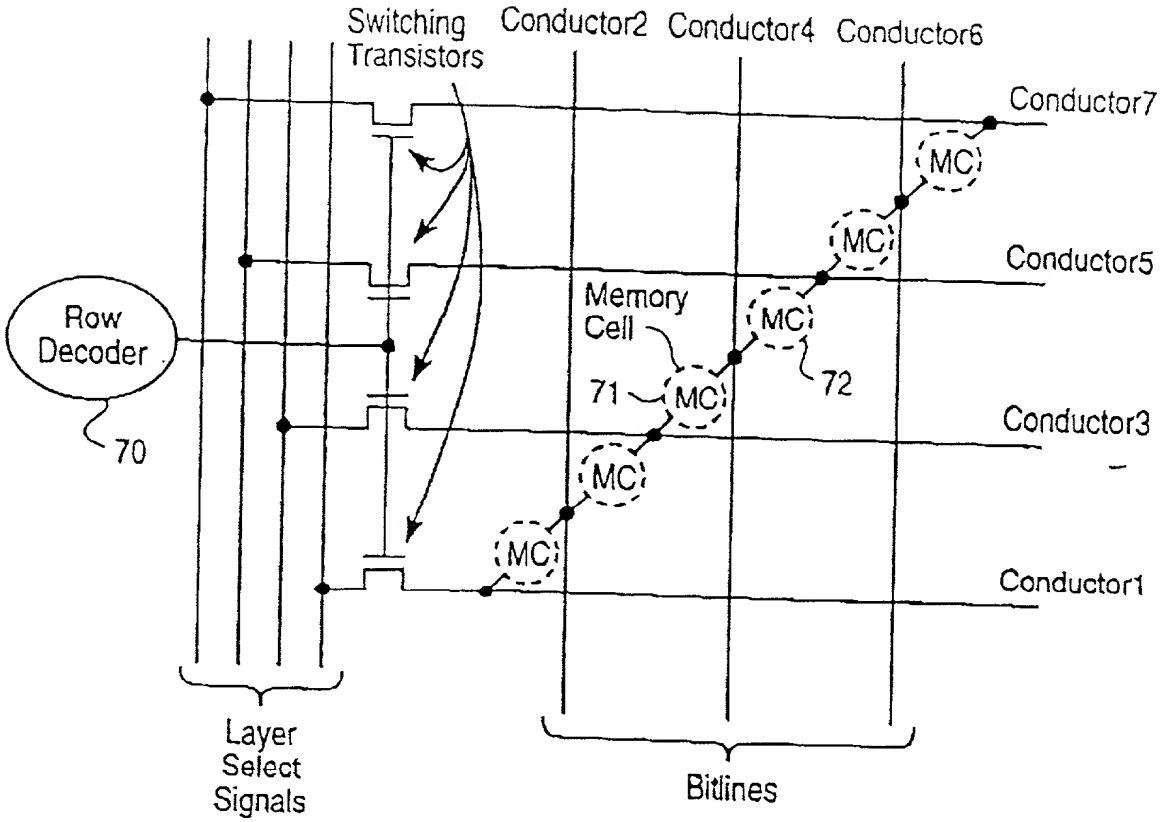

Switching Transistors
Conductor2
Conductor4
Conductor6
Conductor7
Conductor5
Conductor3
Conductor1
Row Decoder
70
Memory Cell
71
72
MC
Layer Select Signals
Bitlines

FIG. 10(a)

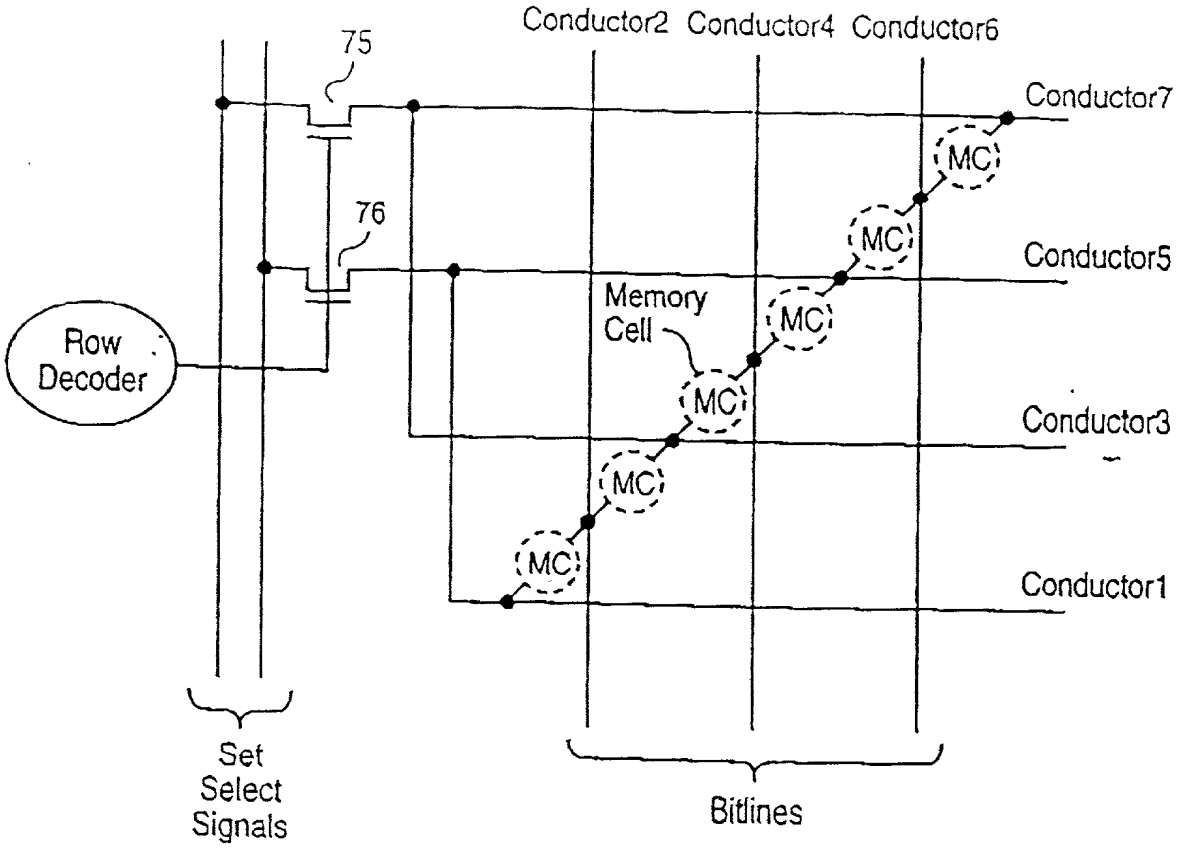

Conductor2
Conductor4
Conductor6
75
Conductor7
MC
76
MC
Conductor5
Memory
Cell
Row
Decoder
MC
MC
Conductor3
MC
MC
Conductor1
Set
Select
Signals
Bitlines

FIG. 10(b)

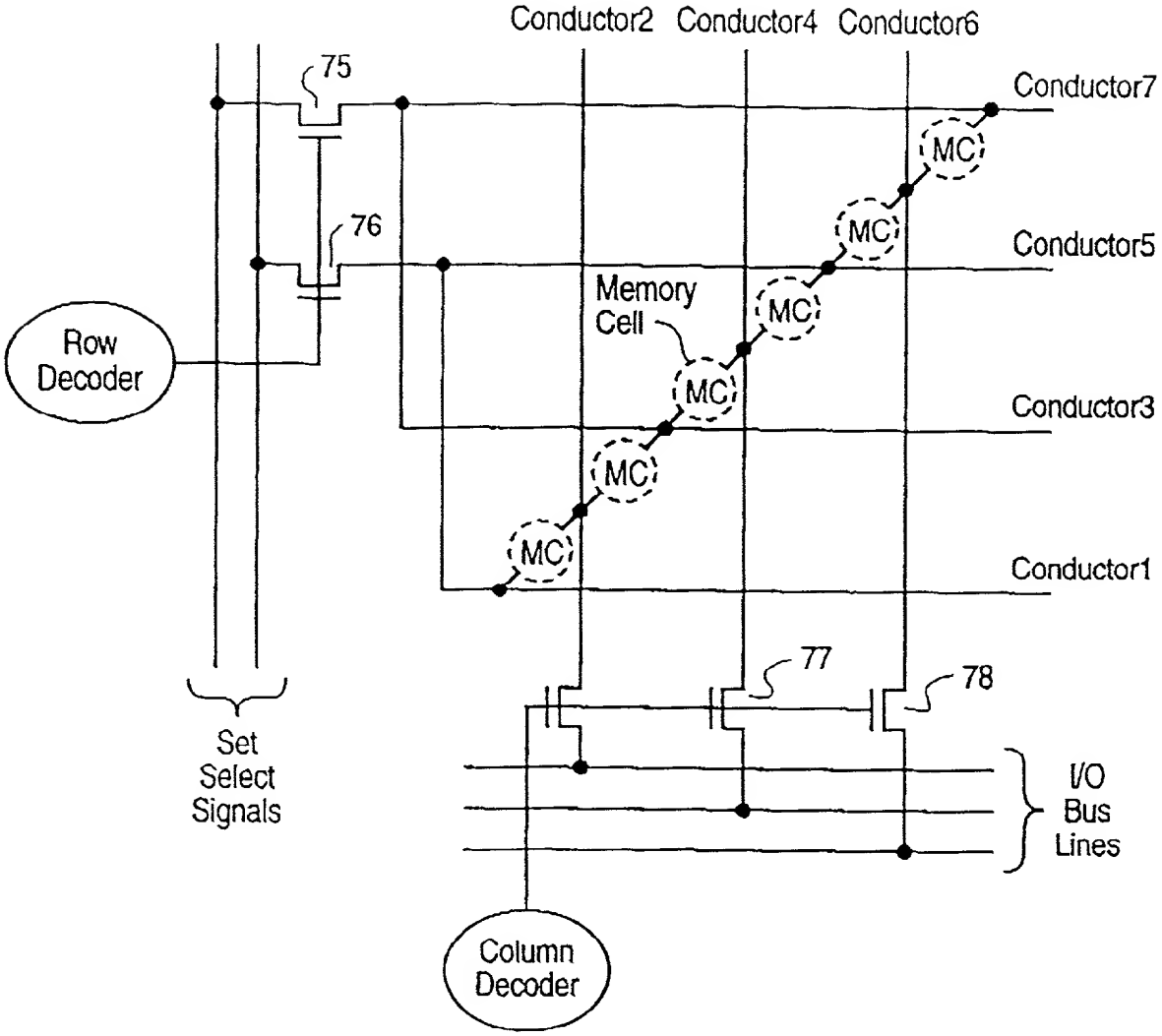

Conductor2
Conductor4
Conductor6
75
Conductor7
MC
76
MC
Conductor5
Memory
Cell
MC
Row
Decoder
MC
Conductor3
MC
MC
Conductor1
77
78
Set
Select
Signals
I/O
Bus
Lines
Column
Decoder

FIG. 11

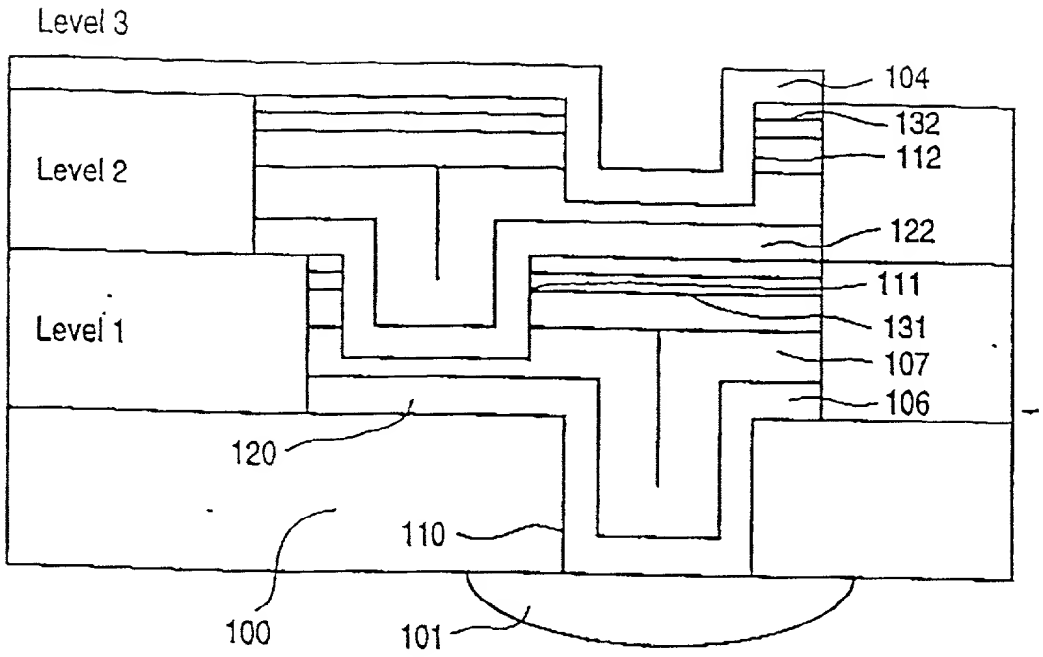

Level 3
Level 2
Level 1
104
132
112
122
111
131
107
106
120
110
100
101

FIG. 12

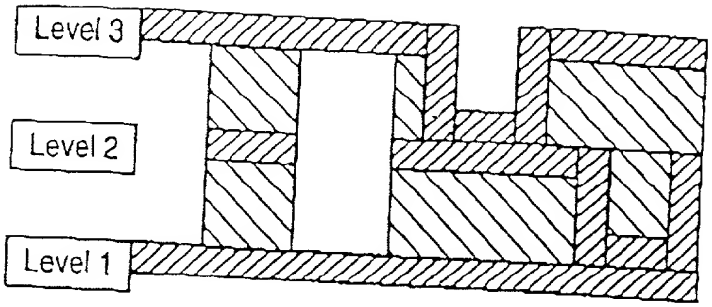


FIG. 13(a)

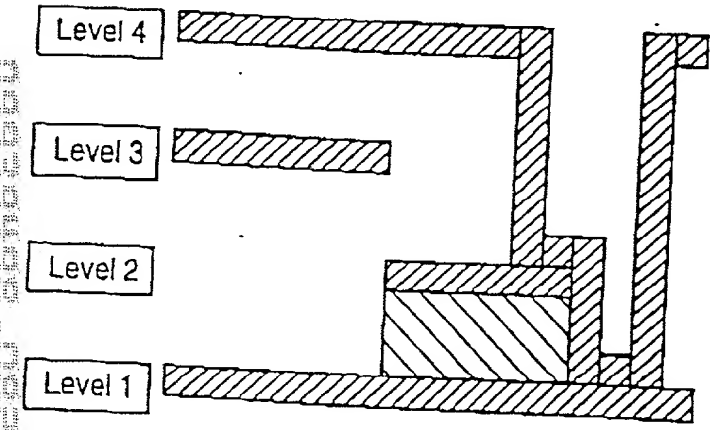


FIG. 13(b)

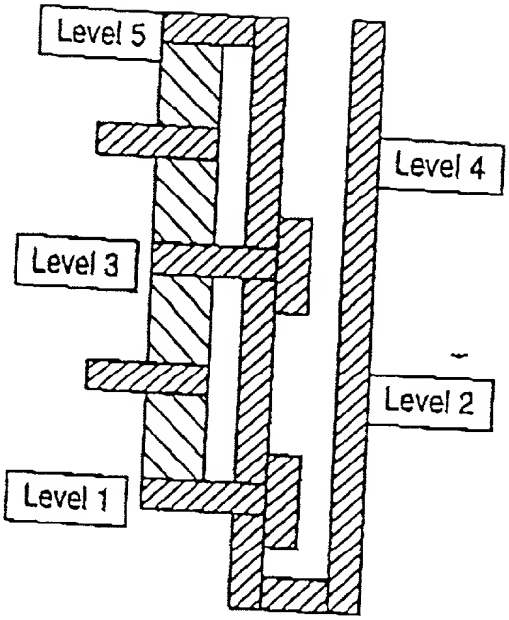


FIG. 13(c)

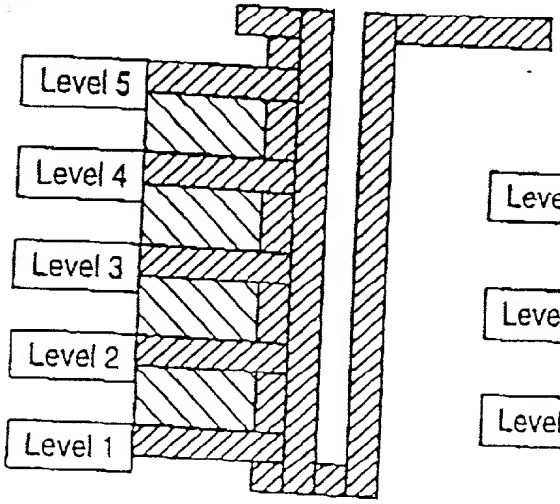


FIG. 13(d)

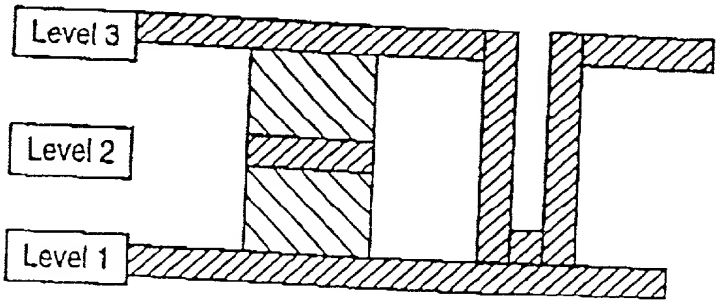


FIG. 13(e)